STATUS OF InP HEMT TECHNOLOGY FOR MICROWAVE RECEIVER APPLICATIONS (INVITED)

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ABSTRACT

The current status of InP-based high electron mobility transistor (HEMT) technology for low noise amplification at frequencies up to more than 100 GHz is presented. Following a review of recent advances industry-wide in both device and circuit performance, two issues which will pace the rate at which this new technology can be inserted into microwave systems–material/process maturity and long-term reliability–are discussed.

INTRODUCTION

InP-based HEMTs have demonstrated high-frequency characteristics superior to those of any other transistor, including the highest f_{max} (600 GHz, as reported in [1], the highest ft (340 GHz, as reported in [2], the lowest noise figure of any room-temperature receiver technology [3],[4] and the highest efficiency at millimeter-wave frequencies [1],[5]. Consequently, much effort is being directed toward the insertion of circuitry based on InP HEMTs into a variety of microwave and millimeter-wave applications that can benefit from their enhanced performance.

Although the earliest microwave HEMTs were based on the GaAs/AlGaAs material system, it became clear by 1986 that GaAs-based HEMTs with pseudomorphic InGaAs channels provided improved millimeter-wave noise and power performance[6]. These GaAs pseudomorphic HEMTs, or PHEMTs, typically contain InGaAs channels with indium content ranging from 15 to 25%. Also in 1986, Aksun et al. reported a 1 µm HEMT with a 53% indium InGaAs channel, *fabricated on an InP substrate,* that exhibited 50% higher f_{max} and f_t than a GaAs-based PHEMT of similar geometry[7]. In 1988, the superior noise performance of InP-based HEMTs was demonstrated convincingly at millimeter-wave frequencies using short-gate devices [8].

The unequaled performance of the InP-based HEMT arises directly from the intrinsic properties of the InAlAs/InGaAs material system, where the high indium content (typically 53-80%) InGaAs channel possesses high electron mobility and velocity, and the large conduction band discontinuity at the InGaAs/InAlAs heterojunction permits high two-dimensional electron gas (2DEG) densities to be obtained, resulting in high current and transconductance. It is the high transconductance of the InP HEMT which is most directly responsible for its increased operating frequency and excellent gain-bandwidth properties. Transconductance values as high as 1500 - 1700 mS/mm have been reported [2],[9], and typical 0.1 µm InP low noise HEMTs exhibit g_m of 800-1000 mS/mm, compared with 600 mS/mm for comparable GaAs PHEMTs.

The cross-section of a typical InP-based HEMT is shown in Figure 1. As is the case with GaAs-based HEMTs, T-shaped TiPtAu gates and silicon nitride passivation have become the industry standards.

The indium mole fraction employed in the channel is normally 53%, allowing the InGaAs to be lattice-matched to the underlying material, but pseudomorphic InGaAs channels with up to 80% indium content continue to be investigated for the further improvement in performance expected based on theoretical considerations. In practice, the best noise performance has been obtained for devices with indium content of 53-60% [3],[4],[8],[10],[11]. The highest values of current gain cutoff frequency f_t have been observed with 80% indium InGaAs channels [2],[12], but these devices have failed to exhibit improved noise performance. Maximum frequency of oscillation f_{max} is a more relevant figure of merit for a microwave transistor than f_t because it relates to power gain, the gain of interest in a high frequency amplifier. We have observed the highest f_{max}, a record 600 GHz, with a 68% indium pseudomorphic InGaAs channel [1].

DEVICE NOISE PROPERTIES

Table 1 summarizes the best reported noise performance measured for InP HEMT devices at frequencies from 18 to 94 GHz. As seen in the table, there have now been several reports of InP HEMTs with noise figure less than 1 dB at 60 GHz, including two reports of devices passivated suc-

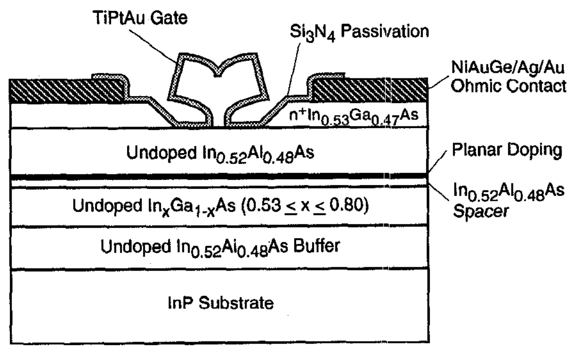

Figure 1. Cross-section of typical InP-based low noise HEMT.

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cessfully with minimal degradation in noise figure [3],[11]. In general, we find that measured device minimum noise figures in the 18 to 94 GHz range follow the frequency dependence proposed by Fukui, that is,

$$F_{min}\,(\text{dB}) = 10 \log (1+cf)$$

Where c is a constant and f is the frequency [14]. As compared with GaAs-based PHEMTs, InP HEMTs offer not only significantly lower noise figure, but typically provide 1-2 dB higher associated gain, which helps to further improve amplifier noise figure by reducing second stage noise contribution. Since InP HEMT minimum noise figure is obtained at a much lower drain bias of 1.0V, compared with 2.0-2.5V for a typical GaAs PHEMT, both DC power consumption and 1 dB gain compression point are significantly lower for InP HEMTs than for PHEMTs (as reported in [17], P_{1dB} was found to be 5-6 dB lower for a W-band InP HEMT). However, this reduction in P_{1dB} (and therefore 3OIP) of a multi-stage amplifier can be recovered by increasing the drain voltage or gate periphery of the output stage device or by adopting a device structure with better power handling properties (see, for example, [1]).

LOW NOISE AMPLIFIERS

A variety of high performance InP HEMT low noise amplifiers (LNAs) have been reported at frequencies ranging from 2 to 140 GHz. These include both hybrid (MIC) amplifiers based on discrete transistors as well as MMICs. In general, the hybrid circuit implementation is used for applications requiring the lowest noise figure and limited in volume, while MMICs are preferred for applications requiring small size (e.g. phased arrays), low production cost in moderate to high volume, and/or excellent repeatability (unit-to-unit tracking).

Figure 2 shows the noise figure achievable in both hybrid and MMIC LNAs over relatively narrow bandwidths (5-10%) using typical passivated 0.1 μm InP HEMTs. Although the hybrid and MMIC LNAs would appear to have identical noise figures (since only one curve is shown for both), the hybrid LNA noise figure is in fact lower since it is referred to the input connector, and therefore includes transition and isolator losses, while the MMIC noise figure shown represents only chip-level performance.

We have reported hybrid LNAs at V- and W-band [4],[15],[16],[17], including a 2-stage amplifier with 1.7 dB noise figure and 17 dB gain at 62 GHz and a 3-stage design with 3.2 dB noise figure and 17 dB gain at 94 GHz. Additional InP HEMT hybrid amplifiers have been reported by others at V-, W- and D-band [18],[19].

A summary of low noise InP HEMT MMICs reported over the past six years is presented in Table 2. MMIC noise figures presently range from less than 0.5 dB at 2 GHz to approximately 3 dB at 94 GHz, and continue to improve. Of particular significance is the W-band MMIC, shown in Figure 3, which exhibited 3.3 dB minimum noise figure at 92 GHz and less than 5.0 dB noise figure across the full 75-110 GHz band (a 35 GHz bandwidth). Also of significance is the 142 GHz MMIC shown in Figure 4; this MMIC represents the highest frequency amplifier demonstrated to date with any transistor technology. In general, one can expect

Ref.	Year Reported	Freq. (GHz)	Gate Length (μm)	Passivation	Noise Figure (dB)	Associated Gain (dB)
[13]	1990	18	0.15	—	0.3	17.1
[8]	1988	60	0.2	—	0.9	8.7
[3]	1994	60	0.1	—	0.7	8.6
[3]	1994	60	0.1	Si_3N_4	0.8	7.6
[11]	1994	60	0.15	SiON	0.9	7.0
[4]	1991	94	0.1	—	1.2	7.2
[10]	1992	94	0.1	—	1.3	8.2

Table 1. Best reported InP low noise HEMTs. In all cases, performance shown is device performance, corrected appropriately for fixture and setup losses.

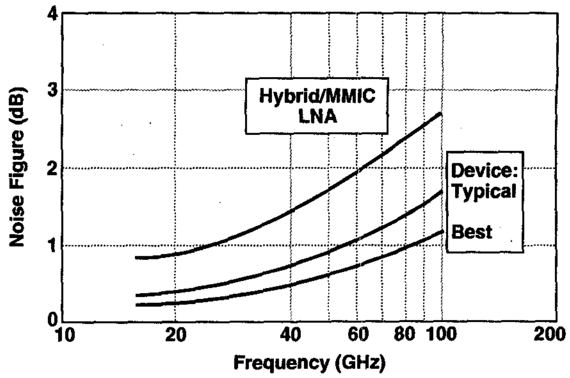

Figure 2. Noise figure achievable in multistage, narrowband LNAs using typical passivated 0.1 μm InP HEMTs. Single-device noise figure is also shown.

Ref.	Year Reported	Freq. (GHz)	# of Stages	Minimum NF (dB)	Gain (dB)	NF over Band (dB)
[20]	1993	2.3-2.5	3	0.4	35	0.5 max.
[21]	1993	7-11	2	1.0	21	1.2 max.
[22]	1995	19-22	3	1.1	38	1.2 max.
[23]	1993	43-46	2	—	25	2.3 ave.
[24]	1995	43-46	3	1.9	22	2.0 ave.
[25]	1994	50	2	2.8	9	—
[19]	1990	63	2	3.0	18	—
[26]	1992	56-60	2	3.2	15	4.2 ave.
[27]	1993	56-64	3	2.7	25	3.0 ave.
[24]	1995	58-62	2	2.2	16	2.3 ave.
[28]	1993	75-110	3	3.3	11	5.0 max.
[29]	1993	75-110	4	6.0	23	—
[30]	1995	92-96	3	3.3	20	4.4 max.
[31]	1994	120-124	2	—	11	—
[32]	1995	142	2	—	9	—

Table 2. Summary of best reported InP HEMT MMIC LNAs.

to see continued progress toward further reduction in MMIC noise figures and increased operating frequencies.

Because of their high gain, InP HEMTs have been used to produce MMIC distributed amplifiers with decade or greater bandwidths and high operating frequencies [33]-[37]. The MMIC shown in Figure 5 demonstrated 5 dB gain from 5 to 100 GHz, the largest bandwidth of any MMIC reported to date. InP HEMTs are also finding application in cryogenic receivers used for radio astronomy: they exhibit the best cryogenic noise performance of any transistor, and have been integrated into receivers that are expected to be competitive with SIS technology at frequencies up to 100 GHz [38]-[40].

MATERIAL AND PROCESS MATURITY

InP HEMT MMICs currently cost more than GaAs-based MMICs for a variety of reasons. InP wafers are smaller (2 and 3-inch vs. 3, 4 and 6-inch for GaAs) and more costly (for 3-inch substrates, \$750-1000 vs. \$130-160 for GaAs). Most InP HEMT device and MMIC fabrication is now carried out on 2-inch wafers, but there is effort underway to scale the processes to 3-inch wafers.

InP MMIC DC and RF yields are generally lower than GaAs today due to less mature processing technology, but this is improving. Probably the single most important process parameter controlling yield and uniformity across large wafers is the gate recess depth. Several workers have recently reported the use of selective gate recess etching techniques that significantly improve InP HEMT process uniformity [9],[11],[41]. In [41], for example, Enoki et al. report a threshold voltage standard deviation of 16 mV across a 2-inch wafer, corresponding to a gate recess depth variation of *only a few angstroms.*

Even though InP HEMT process yields are expected to reach levels comparable to GaAs, MMICs produced on InP substrates will almost certainly always be higher in cost than GaAs MMICs, and will therefore be used only where performance requirements mandate their use. A promising new development that could allow the production of InP HEMT MMICs at essentially *the same* cost as GaAs MMICs is the metamorphic InAlAs/InGaAs HEMT, in which the InP HEMT epitaxial layers are grown directly on GaAs substrates and special buffer layer structures are used to accommodate the large lattice mismatch. Recently, metamorphic InAlAs/InGaAs HEMTs have demonstrated both DC transconductance [42] and 12 GHz noise figure [43] comparable to that achieved on InP substrates. The impact of the relatively large threading dislocation density of the top layers (10^6-10^7 cm^{-2}) on InP HEMT MMIC yield and reliability, however, has not yet been fully assessed.

RELIABILITY

Even the highest performance device is of little use if its reliability fails to meet application requirements. Satellite applications are perhaps the most demanding in terms of required operating lifetime, with a typical MTTF requirement of 10^7 hours at a channel temperature of 80°C. As reported in [44], InP HEMT MTTF is lower than that of GaAs PHEMTs, but the MTTF of more than 10^8 hours at 100°C easily meets even stringent satellite lifetime requirements.

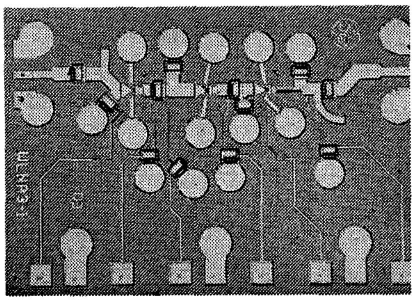

Figure 3. 3-stage 75-110 GHz MMIC (from [28]).

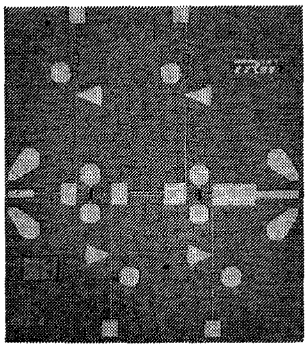

Figure 4. 2-stage 142 GHz MMIC (from [32]).

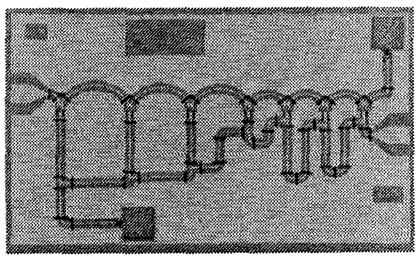

Figure 5. 5-100 GHz MMIC distributed amplifier (from [33]).

Passivation is desirable to reduce InP HEMT sensitivity to environmental effects (particularly humidity). Thin layers (typically 500Å) of silicon nitride and SiON have been found to produce minimal degradation in the performance of millimeter wave InP low noise HEMTs [3],[13],[30], but these layers are probably too thin to be pinhole-free and so thicker passivation layers are likely to be needed for non-hermetic applications. In addition, it has been reported that InP HEMTs with TiPtAu gate metallization degrade more rapidly than GaAs PHEMTs in the presence of hydrogen which can accumulate within hermetically sealed packages [46], and work is progressing throughout the industry both to modify the device structure to minimize its hydrogen sensitivity and to reduce the hydrogen partial pressure within the package (see, for example, [47]).

FUTURE TRENDS AND SUMMARY

InP HEMTs have demonstrated the best high frequency characteristics of any transistor produced to date, and possess significant potential for further improvement. The 600 GHz f_{max} device reported in [1] exhibits useful gain at frequencies up to 200-300 GHz; with additional optimization of the device design, an f_{max} of 1 THz is likely, enabling for the first time a host of military and commercial applications at frequencies beyond 100 GHz. Below 100 GHz, InP HEMTs will find widespread use in a number of receiver applications, their insertion being limited only by the speed with which their manufacturability can be improved.

ACKNOWLEDGMENT

The author gratefully acknowledges the assistance of Marion Pospieszalski, Cindy Yuen and Huei Wang in assembling the material for this paper. In addition, the contributions of coworkers involved in InP HEMT development at the Lockheed Martin Electronics Laboratory, including P.C. Chao, K.H.G. Duh, P. Ho, S.M.J. Liu, S. Wang, M. Kao and J.M. Ballingall are recognized.

REFERENCES

[1] P.M. Smith, et al., "W-Band High Efficiency InP-Based Power HEMT with 600 GHz f_{max}," *IEEE Microwave and Guided Wave Lett.*, vol. 5, no. 7, pp. 230-232, July 1995.

[2] L.D. Nguyen, et al., "50 nm Self-Aligned Gate Pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," *IEEE Trans. Electron Devices*, vol. 39, pp. 2007-2014, 1992.

[3] M.Y. Kao, et al., "An Extremely Low-Noise InP-Based HEMT With Silicon Nitride Passivation," *IEDM Tech. Dig.*, pp. 907-910, 1994.

[4] K.H.D. Duh, et al., "A Super Low-Noise 0.1 μm T-Gate InAlAs-InGaAs-InP HEMT," *IEEE Microwave And Guided Wave Lett.*, vol. 1, no. 5, pp. 114-116, May 1991.

[5] P. Ho, et al., "60 GHz Power Performance of 0.1 μm Gate-Length InAlAs/InGaAs HEMTs," *6th Int. Conf. on InP and Related Materials*, pp. 411-414, 1994.

[6] T. Henderson, et al., "Microwave Performance of a Quarter-Micrometer Gate Low-Noise Pseudomorphic InGaAs/AlGaAs Modulation-Doped Field Effect Transistor", *IEEE Electron Device Lett.*, vol. 7, pp. 649-651, December 1986.

[7] M.I. Aksun, et al., et al., "High Frequency Modulation Doped Field Effect-Transistors in InAlAs/InGaAs/InP Material System," *IEDM Tech. Dig.*, pp. 822-823, 1986.

[8] U.K. Mishra, et al., "Microwave Performance of AlInAs-GaInAs HEMTs with 0.2 and 0.1 μm Gate Length," *IEEE Electron Device Lett.*, vol. 9, no. 12, pp. 647-649, Dec. 1988.

[9] T. Enoki, et al., "Device Technologies for InP-Based HEMTs and Their Application to IC's," *GaAs IC Symp. Dig.*, pp. 337-339, 1994.

[10] D.C. Streit, et al., "MBE Growth and Characterization of Lattice-Matched and Pseudomorphic InGaAs/InAlAs/InP HEMTs," *4th Int. Conf. on Indium Phosphide and Related Materials*, pp. 682-684, April 1992.

[11] N. Yoshida, et al., "A Super Low Noise V-Band AlInAs/InGaAs HEMT Processed By Selective Wet Gate Recess Etching," *IEEE MTT-S Digest*, pp. 645-648, 1994.

[12] M. Wojtowicz, et al., "0.10 μm Graded InGaAs Channel InP HEMT with 305 GHz f_t and 340 GHz f_{max}," *IEEE Electron Device Lett.*, vol. 15, pp. 477-479, Nov. 1994.

[13] P.C. Chao, et al., "W-Band Low-Noise InAlAs/InGaAs Lattice-Matched HEMTs," *IEEE Electron Device Lett.*, vol. 11, no. 1, pp. 59-62, Jan. 1990.

[14] H. Fukui, "Optimal Noise Figure of Microwave GaAs MESFETs," *IEEE Trans. Elec. Dev.*, pp. 1032-1037.

[15] K.H.G. Duh, et al., "W-Band InGaAs HEMT Low Noise Amplifiers," *IEEE MTT-S Digest*, pp. 595-598, 1990.

[16] K.H.G. Duh, et al., "High-Performance InP-Based HEMT Millimeter-Wave Low-Noise Amplifiers," *IEEE MTT-S Digest*, pp. 805-808, 1989.

[17] P.M. Smith, et al., "Microwave InAlAs/InGaAs/InP HEMTs: Status and Applications," *2nd Int. Conf. on InP and Related Materials*, pp. 39-43, April 1990.

[18] S. Vaughn, et al., "High Performance V-Band Low Noise Amplifiers," *IEEE MTT-S Digest*, pp. 801-804, 1989.

[19] P.D. Chow, et al., "W-Band and D-Band Low Noise Amplifiers Using 0.1 Micron Pseudomorphic InAlAs/InGaAs/InP HEMTs," *IEEE MTT-S Digest*, pp. 807-810, 1992.

[20] S.E. Rosenbaum, et al., "A 2 GHz Three-Stage AlInAs-GaInAs-InP HEMT MMIC Low-Noise Amplifier," *IEEE Microwave and Guided Wave Lett.*, vol. 3, no. 8, pp. 265-267, August 1993.

[21] S.E. Rosenbaum, et al., "A 7 to 11 GHz AlInAs/GaInAs/InP MMIC Low Noise Amplifier," *IEEE MTT-S Dig.*, pp. 1103-1104, 1993.

[22] K.H.G. Duh, private communication. Presented at IEEE MILCOM Conf., San Diego, CA, Nov. 1995.

[23] D.C.W. Lo, et al., " A High-Performance Monolithic Q-Band InP-Based HEMT Low-Noise Amplifier," *IEEE Microwave and Guided Wave Lett.*, vol. 3, no. 9, pp. 299-301, Sept. 1993.

[24] R. Isobe, et al., "Q- and V-Band MMIC Chip Set Using 0.1 μm Millimeter-Wave Low Noise InP HEMTs," *IEEE MTT-S Digest*, pp. 1133-1136, 1995.

[25] Y. Umeda, et al., "Sensitivity Analysis of 50 GHz MMIC LNA On Gate-Recess Depth With InAlAs/InGaAs/InP HEMTs," *IEEE MTT-S Digest*, pp. 123-126, 1994.

[26] R.T. Webster, et al., "Monolithic InP HEMT V-Band Low-Noise Amplifier," *IEEE Microwave and Guided Wave Lett.*, vol. 2, no. 6, pp. 236-238, June 1992.

[27] R. Lai, et al., "A High Performance And Low DC Power V-Band MMIC LNA Using 0.1 μm InGaAs/InAlAs/InP HEMT Technology," *IEEE Microwave and Guided Wave Lett.*, vol. 3, no. 12, pp. 447-449, Dec. 1993.

[28] K.H.D. Duh, et al., "Advanced Millimeter-Wave InP HEMT MMICs," *5th Int. Conf. on InP and Related Materials*, pp 493-496, April 1993.

[29] H. Wang, et al., "A Monolithic 75-110 GHz Balanced InP-Based HEMT Amplifier," *IEEE Microwave And Guided Wave Lett.*, vol. 3, no. 10, pp. 381-383, Oct. 1993.

[30] G.I. Ng, et al., "A Fully Passivated Ultra Low Noise W-Band Monolithic InGaAs/InAlAs/InP HEMT Amplifier," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, pp. 63-65, 1995.

[31] R. Lai. et al., "A Monolithically Integrated 120 GHz InGaAs/InAlAs/InP HEMT Amplifier," *IEEE Microwave And Guided Wave Lett.*, vol 4, no. 6, pp. 194-195, June 1994.

[32] H. Wang, et al., "A 140 GHz Monolithic Low Noise Amplifier," *IEEE Microwave and Guided Wave Lett.*, vol. 5, no. 5, pp. 150-152, May 1995.

[33] R. Majidi-Ahy, et al., "5-100 GHz InP Coplanar Waveguide MMIC Distributed Amplifier," *IEEE Trans. MTT*, vol. 38, no. 12, pp. 1986-1993, Dec. 1990.

[34] C. Yuen, et al, "Ultra-High Gain, Low Noise Monolithic InP HEMT Distributed Amplifier from 5 to 40 GHz, *Elec. Letters*, vol. 26, no. 8, p. 515, April 1990.

[35] C. Yuen, et al, "Monolithic InP Cascode HEMT Distributed Amplifier From 5 to 40 GHz," *Elect. Letters*, vol. 26, no. 17, p. 1411, Aug. 1990.

[36] C. Yuen, et al., "High-Gain, Low-Noise Monolithic HEMT Distributed Amplifiers Up To 60 GHz," *IEEE Trans. MTT*, vol. 38, no. 12, pp. 2016-2017, Dec. 1990.

[37] T. Shibata, et al., "60 GHz-Bandwidth Distributed Baseband Amplifier IC in a Package Optimized For Isolation," *IEEE ISSCC Dig.*, pp. 180-181, 1994.

[38] M.W. Pospieszalski, et al., "Millimeter-Wave, Cryogenically Coolable Amplifiers Using AlInAs/ GaInAs/InP HEMTs," *IEEE MTT-S Digest*, pp. 515-518, 1993.

[39] M.W. Pospieszalski, et al., "Very Low Noise and Low Power Operation of Cryogenic AlInAs/GaInAs/InP HFETs," *IEEE MTT-S Digest*, pp. 1345-1346, 1994.

[40] M.W. Pospieszalski, et al., "Q- and E-Band Cryogenically-Coolable Amplifiers Using AlInAs/GaInAs/InP HEMTs," *IEEE MTT-S Digest*, pp. 1121-1124, 1995.

[41] T. Enoki, et al., "0.1 μm InAlAs/InGaAs HEMTs With An InP-Recess-Etch Stopper Grown By MOCVD," *7th Int. Conf. on InP and Related Materials*, pp. 81-84, 1995.

[42] K. Higuchi, et al., "First High Performance InAlAs/InGaAs HEMTs on GaAs Exceeding That on InP," *IEEE IEDM Tech. Dig.*, pp. 891-894, 1994.

[43] H. Rohdin, et al., "Low-Noise, High-Speed GaInAs/AlInAs 0.1 μm MODFETs and High-Gain/Bandwidth Three-Stage Amplifier Fabricated on GaAs Substrate," *7th Int. Conf. on InP and Related Materials*, pp. 73-76, 1995.

[44] P.M. Smith, et al., "Application of GaAs and InP-Based HEMT Technology to MILSATCOM Systems," *IEEE MILCOM Conf. Dig.*, pp. 731-736, 1995.

[45] P.C. Chao, et al., "HEMT Degradation in Hydrogen Gas," *IEEE Electron Device Lett.*, vol. 15 no. 5, pp. 151-153, May 1994.

[46] Y. Saito, et al., "Hydrogen Degradation of GaAs MMICs and Hydrogen Evolution in the Hermetic Package," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, pp. 119-122, 1995.